Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device provided with a memory cell including a first driver transistor, a second driver transistor, a first transfer transistor, a second transfer transistor, a first load transistor and a second load transistor, the semiconductor device comprising:

a first gate-gate electrode layer including a gate electrode of the first load transistor and a gate electrode of the first driver transistor;

a second gate-gate electrode layer including a gate electrode of the second load transistor and a gate electrode of the second driver transistor;

a first drain-drain wiring layer which forms a part of a connection layer that electrically connects a drain region of the first load transistor and a drain region of the first driver transistor;

a second drain-drain wiring layer which forms a part of a connection layer that electrically connects a drain region of the second load transistor and a drain region of the second driver transistor;

a first drain-gate wiring layer which forms a part of a connection layer that electrically connects the first gate-gate electrode layer and the second drain-drain wiring layer;

a second drain-gate wiring layer which forms a part of a connection layer that electrically connects the second gate-gate electrode layer and the first drain-drain wiring layer; and

a first active region in which the first load transistor is provided,

wherein the first drain-gate wiring layer and the second drain-gate wiring layer are located in different layer levels, respectively, and

wherein a first protruded active region is provided in a manner to protrude from an end portion of the first active region[[.]] , and

wherein the second drain-gate wiring layer includes a lower layer of the second drain-gate wiring layer and an upper layer of the second drain-gate wiring layer; and

wherein the upper layer is located in a layer over the lower layer, and electrically connected to the lower layer; and

wherein the first gate-gate electrode layer, the second gate-gate electrode layer and the first drain-gate wiring layer are located in a first conductive layer level; and

wherein the first drain-drain wiring layer, the second drain-drain wiring layer and the lower layer are located in a second conductive layer level; and

wherein the upper layer is located in a third conductive layer level.

2. (Original) The semiconductor device according to claim 1, wherein the first protruded active region is provided in a manner to protrude on a side opposite to a side where the first and second driver transistors are provided.

3. (Original) The semiconductor device according to claim 1, wherein a part of the first active region and the first protruded active region form an L-shape.

4. (Original) The semiconductor device according to claim 1, comprises:

a second active region in which the second load transistor is provided; and

a second protruded active region provided in a manner to protrude from an end portion of the second active region.

5. (Original) The semiconductor device according to claim 4, wherein the second protruded active region is provided in a manner to protrude on a side opposite to a side where the first and second driver transistors are provided.

6. (Original) The semiconductor device according to claim 4, wherein a part of the second active region and the second protruded active region form an L-shape.

7. (Original) The semiconductor device according to claim 1,

wherein the first drain-gate wiring layer is electrically connected to the second drain-drain wiring layer through a contact section, and

wherein the second drain-gate wiring layer is electrically connected to the second gate-gate electrode layer through a contact section, and electrically connected to the first drain-drain wiring layer through a contact section.

8. (Original) The semiconductor device according to claim 1, wherein the first drain-gate wiring layer is located in a layer lower than the second drain-gate wiring layer.

9. (Original) The semiconductor device according to claim 1, wherein the first drain-gate wiring layer is located in a layer in which the first gate-gate electrode layer is provided.

10. (Original) The semiconductor device according to claim 1, wherein the second drain-gate wiring layer is formed across a plurality of layers.

11. (Cancelled)

12. (Currently Amended) The semiconductor device according to claim 10, wherein the upper layer is electrically connected to the lower layer through a contact section.

13. (Cancelled)

14. (Currently Amended) The semiconductor device according to claim 10, wherein the second conductive layer level is a nitride layer of a refractory metal.

15. (Currently Amended) The semiconductor device according to claim 10, wherein the second conductive layer has a thickness of 100 nm to 200 nm.

16. (Cancelled)

17. (Currently Amended) A memory system provided with the semiconductor device defined in any one of claims 1-10, 12, and 14-15.

18. (Currently Amended) An electronic apparatus provided with the semiconductor device defined in any one of claims 1-10, 12, and 14-15.